1. A method to form an elongated solder bump, comprising:

providing a first substrate and forming thereon a first solder bump;

providing a second substrate and forming thereon a second solder bump;

positioning said first and second solder bumps to be in positional and angular alignment relative to one another, said solder bumps being separated by a first distance and said substrates being separated by a second distance;

heating both solder bumps till they melt;

then reducing said first distance until the molten solder bumps merge into a single solder bump;

while maintaining single solder bump in its molten state, increasing said second distance between substrates thereby lengthening said single solder bump and forming said elongated solder bump;

terminating the step of increasing said second distance when said elongated solder bump achieves a desired aspect ratio then allowing it to solidify through cooling; and

separating the elongated solder bump from said second substrate only.

2. The method recited in claim 1 wherein said desired aspect ratio is at least 2

3. A method to form an elongated solder bump, comprising:

providing a first substrate and forming thereon a solder bump;

providing a second substrate and forming thereon a wettable solder pad;

positioning said solder bump and solder pad to be in positional and angular alignment relative to one another, said solder bump and solder pad being separated by a first distance and said substrates being separated by a second distance;

heating said solder bump till it melts;

then reducing said first distance until the molten solder bump contacts and wets the solder pad;

while maintaining said solder bump in its molten state, increasing said second distance between substrates thereby lengthening said solder bump and forming an elongated solder bump;

terminating the step of increasing said second distance when said elongated solder bump achieves a desired aspect ratio and then allowing it to solidify through cooling; and

separating the elongated solder bump from said second substrate only.

4. The method recited in claim 3 wherein said first distance that initially separates the solder bumps is about 0.5 mm.

5. A process to manufacture a wafer level circuit package, comprising:

providing a plurality of integrated circuits on a functional wafer, including a top layer of insulation having access holes for making electrical contact to said integrated circuits;

forming a first pattern of contact pads whereby there is one contact pad over each of said access holes;

providing a master wafer and depositing thereon a sacrificial layer;

forming, on said sacrificial layer, a second pattern of contact pads that is a mirror image of said first pattern;

forming a solder bump on each one of the contact pads;

positioning said master and functional wafers so that each solder bump on the master wafer is in vertical alignment with a solder bump on the functional wafer, said solder bumps being separated by a first distance and said wafers being separated by a second distance;

heating all solder bumps till they melt;

then reducing said first distance until the aligned molten solder bumps touch one another and form merged solder bumps;

while maintaining all solder in its molten state, increasing said second distance between substrates thereby lengthening said merged solder bumps, forming therefrom elongated solder bumps;

terminating the step of increasing said second distance when said elongated solder bumps achieve a desired aspect ratio and then allowing them to solidify through cooling; and

selectively removing said sacrificial layer from said master wafer, thereby separating all elongated solder bumps from only said master wafer,

6. The process described in claim 5 wherein said sacrificial layer is selected from the group consisting of high temperature polymers, amorphous silicon, polysilicon, and silicon oxide.

7. The process described in claim 5 wherein said sacrificial layer is deposited to a thickness between about 0.2 and 1 microns.

8. The process described in claim 5 wherein the step of selectively removing said sacrificial layer of amorphous silicon further comprises etching in Xenon difluoride for between about 2 and 60 minutes at a temperature between about 25 and 34 C.

9. The process described in claim 5 further comprising, after said elongated solder bumps no longer contact said master wafer, dicing said functional wafer into individual chips.

10. The process described in claim 9 wherein said chips are attached to a printed circuit board using a solder whose melting point is at least 50 °C below that of said elongated solder bumps.

11. A process to manufacture a wafer level circuit package, comprising:

providing a plurality of integrated circuits on a functional wafer, including a top layer of insulation having access holes for making electrical contact to said integrated circuits;

forming a first pattern of contact pads whereby there is one contact pad over each of said access holes;

providing a master wafer on whose surface is a second pattern of contact pads that is a mirror image of said first pattern;

forming a solder bump on each one of the contact pads;

positioning said master and functional wafers so that each solder bump on the master wafer is in vertical alignment with a solder bump on the functional wafer, said solder bumps being separated by a first distance and said wafers being separated by a second distance;

heating all solder bumps till they melt;

then reducing said first distance until the aligned molten solder bumps touch one another and merge into single solder bumps;

while maintaining all solder bumps in their molten state, increasing said second distance between substrates thereby lengthening each merged solder bump, forming therefrom elongated solder bumps;

terminating the step of increasing said second distance when said elongated solder bumps achieve a desired aspect ratio and then allowing them to solidify through cooling; and

then consuming said master wafer in its entirety whereby said elongated solder bumps are just exposed and remain attached to said functional wafer only.

12. The process described in claim 11 wherein the step of consuming said master wafer further comprises etching it.

13. The process described in claim 11 wherein the step of consuming said master wafer further comprises:

introducing a mechanical stabilization medium between all elongated solder bumps;

grinding and polishing said master wafer until said elongated solder bumps are just exposed; and

then removing said mechanical stabilization medium.

14. The process described in claim 11 wherein said mechanical stabilization medium is a wax.

14a The process described in claim 11 wherein said mechanical stabilization medium is a thermoplastic which may be left on the wafer and serve as a reinforcement to the interconnect when attached to the board.

15. The process described in claim 11 further comprising, after said elongated solder bumps no longer contact said master wafer, dicing said functional wafer into individual chips.

16. The process described in claim 11 wherein said chips are attached to a printed circuit board using a solder whose melting point is at least 50 C below that of said elongated solder bumps.

17. The process described in claim 11 wherein said desired aspect ratio is at least 2.

18. A process to manufacture a wafer level circuit package, comprising:

providing a plurality of integrated circuits on a functional wafer, including a top layer of insulation having access holes for making electrical contact to said integrated circuits;

forming a first pattern of contact pads whereby there is one first contact pad over each of said access holes, each of said first contact pads having a first adhesive strength with respect to said top layer of insulation;

providing a master wafer on whose surface is a second pattern of contact pads that is a mirror image of said first pattern, said second contact pads having a second adhesive strength, with respect to said master wafer surface, that is less than said first adhesive strength;

forming a solder bump on each one of the contact pads;

positioning said master and functional wafers so that each solder bump on the master wafer is in vertical alignment with a solder bump on the functional wafer, said solder bumps being separated by a first distance and said wafers being separated by a second distance;

heating all solder bumps till they melt;

then reducing said first distance until the aligned molten solder bumps touch one another and merge into single solder bumps;

while maintaining all solder bumps in their molten state, increasing said second distance between substrates thereby lengthening said merged solder bumps, forming therefrom elongated solder bumps;

terminating the step of increasing said second distance when a desired aspect ratio of said elongated solder bumps has been achieved and then allowing them to solidify through cooling; and

then separating the master and functional wafers until a separation force that equals said second adhesive strength is achieved whereby all of said elongated solder bumps separate from only said master wafer.

19. The process described in claim 18 wherein said second contact pads are selected from the group consisting of gold, copper, nickel, palladium, tin and silver.

20. The process described in claim 18 wherein said second adhesive strength is less than 50% of a force that initiates damage to said solidified elongated solder bumps.

21. The process described in claim 18 further comprising:

dicing said functional wafer into individual chips and then attaching said chips to a printed circuit board using a solder whose melting point is at least 50 °C below that of said elongated solder bumps.

22. A process to form an elongated solder bump, comprising:

providing flexible laminate of dry film on copper foil;

patterning said dry film thereby exposing said copper foil wherever it is desired to form solder bumps;

coating said copper foil and dry film with solder, said dry film thereby serving as a mask;

aligning and positioning a functional wafer at a distance over said flexible laminate while heat is applied to melt solder bumps on the functional wafer as well as on the flexible laminate;

lowering the functional wafer until all opposing solder bumps are merged;

while maintaining the merged solder in the molten state, raising the functional wafer and thereby stretching the solder;

stopping said raising of the functional wafer when a desired elongated profile of the solder is reached;

while maintaining a separation between the two wafers, cooling the wafer chuck to allow solidification of the stretched solder columns and then releasing all parts from their holders; and

releasing the solder columns from the flexible laminate by chemically etching away the copper foil portion of the flexible laminate.

23. The process described in claim 22 wherein said layer of solder is deposited by printing, plating, jetting or solder ball placement.

24. The process described in claim 22 wherein said flexible laminate is in the form of a roll.

25. A process to manufacture a wafer level circuit package, comprising:

providing a plurality of integrated circuits on a functional wafer, including a top layer of insulation having access holes for making electrical contact to said integrated circuits;

forming a first pattern of contact pads whereby there is one contact pad over each of said access holes;

providing a master wafer on whose surface is a second pattern of contact pads that is a mirror image of said first pattern;

forming a solder bump on each one of the contact pads on said functional wafer;

positioning said master and functional wafers so that each solder bump on the functional wafer is in vertical alignment with a solder pad on the master wafer, said solder bumps and pads being separated by a first distance and said wafers being separated by a second distance;

heating all solder bumps till they melt;

then reducing said first distance until the aligned molten solder bumps touch and wet the solder pads;

while maintaining all solder bumps in their molten state, increasing said second distance between substrates thereby lengthening each of said solder bumps, forming elongated solder bumps;

terminating the step of increasing said second distance when said elongated solder bumps achieve a desired aspect ratio and then lowering the temperature of the master wafer to a hot working temperature of the solder while maintaining the functional wafer at a lower temperature;

while maintaining a temperature gradient in the solder, further separating the master and functional wafers until physical separation of the elongated solder from only said master wafer occurs; and

leveling uneven ends of separated and elongated solder by means of a non-wetting leveling plate.

26. The process described in claim 25 wherein, after the elongated solder bumps have achieved a desired aspect ratio, the functional wafer is cooled to at least 50 °C below the hot working temperature of the solder while the master wafer is brought to the hot working temperature of the solder.

27. The process described in claim 25 wherein the leveling process further comprises:

holding the functional wafer, with free-standing unevenly elongated solder bumps, on the same chuck used for elongation;

maintaining the wafer at a temperature that is at least 50 C below the hot working temperature of the elongated solder; and

lowering the functional wafer so that the elongated solder bumps are pressed against a heated leveling plate, thereby causing them to flatten out and their ends to become co-planar.

28. The process described in claim 25 wherein the leveling plate is heated to the hot working temperature of the solder and its surface is aligned parallel to that of the functional wafer.

29. The process described in claim 25 wherein flattening is such that all the elongated solder bumps have the same height with flat and dovetail-shaped ends.

30. The process described in claim 25 further comprising dicing said functional wafer into individual chips and then attaching said chips to a printed circuit board using a solder whose melting point is at least 50 °C below that of said elongated solder bumps.

31. The process described in 25 wherein the solder that has a lower melting temperature melts and wets the dovetail-shaped solder columns thereby anchoring the elongated solder bumps to the printed circuit board during attachment.